DDR Power Solution Using the ISL6539

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Introduction

The ISL6539 is capable of providing a complete solution for the power requirements of DDRI, DDRII or DDRIII memory systems. The ISL6539 can be configured to operate as a dual switching regulator or as a DDR regulator. This application note will focus on the ISL6539 configured as a DDR regulator. For information on the ISL6539 configured as a dual switching regulator, refer to either the datasheet[1] or to application note AN1278.

As a DDR regulator, the ISL6539 provides control and protection for both the V_{DDQ} and V_{TT} rails while also providing V_{REF} for the DDR system. Both V_{DDQ} and V_{TT} are provided through synchronous buck regulation. V_{REF} is provided via a low current buffer.

The switching frequency is fixed at 300kHz for both the V_{DDQ} and V_{TT} regulators. The two channels can be phase shifted 90° in order to minimize interaction. The ISL6539 incorporates voltage-feed-forward ramp modulation, current mode control, and internal feedback compensation, which provides fast response to input voltage and output load transients.

Protection features include undervoltage and overvoltage protection as well as a programmable overcurrent protection feature that utilizes the $r_{DS(ON)}$ of the lower MOSFET. A more complete description of the ISL6539 can be found in the datasheet.

Quick Start Evaluation

The ISL6539EVAL1 board is shipped ‘ready to use’ right from the box. The box includes this application note, the ISL6539 datasheet, and the evaluation board.

The evaluation board supports testing with laboratory power supplies. Both regulated outputs can be exercised through external loads. There are posts available on the two regulated output rails for drawing a load and/or monitoring the voltages. An LED indicates the status of the PGOOD signal. There are also three scope probe points that allow for in depth analysis and two posts available to monitor the enable signals for either channel. Four jumpers have also been provided for control and monitoring purposes.

Recommended Test Equipment

To test the full functionality of the ISL6539, the following equipment is recommended:

- Two laboratory power supplies
- Two Electronic Loads
- Four-channel Oscilloscope with probes
- Precision Digital Multimeters

CIRCUIT SETUP

Refer to Figure 1 for locations of the jumpers, connectors and components described in the following sections.

JUMPER SETTINGS

There are four jumpers on the board. Shunting jumper JP3 pulls the EN1 pin to VCC and is used to enable Channel 1, which is the V_{DDQ} regulator. Shunting jumper JP4 enables Channel 2, which is the V_{TT} regulator. It should be noted that the input rail for the V_{TT} regulator is the V_{DDQ} rail. If the V_{DDQ} rail is to be disabled and the V_{TT} rail enabled, then the V_{DDQ} rail must be energized from an external power supply and a 0.01µF capacitor should be installed in location C21 for the V_{TT} rail to soft-start properly. C21 is the soft-start capacitor for the V_{TT} rail, as shown in the schematic.

Jumper JP1 can be used to monitor the ISL6539 bias current by connecting an ammeter to the two jumper pins. If the bias current is not being monitored, this jumper must be shunted.

Jumper JP5 is used to set the phase angle between the two switching regulators. Refer to Figure 1 for the jumper positions relating to the desired phase angle. Table 1 also provides a detailed description of the jumper descriptions and positions.

JUMPER	POSITION	FUNCTION
JP1	Shunted	An AmpMeter may be connected across these pins to measure IC and GATE Drive current
JP3	Shunted	CH1 enabled
	Removed	CH1 disabled
JP4	Shunted	CH2 enabled
	Removed	CH2 disabled
JP5	Toward VINPRG	This will tie VIN pin to the input voltage for feed forward. It will also program CH2 PWM to phase lag CH1 by 90°
	Away from VINPRG	This will tie VIN pin to GND, disabling input voltage feed forward, and will also program in phase PWM for CH1 and CH2

TABLE 1. DETAILED DESCRIPTION OF THE JUMPER SETTINGS

CONNECTING LOADS

Loads should only be connected to the V_{DDQ} and V_{TT} rails.

Loading V_{DDQ}: Connect the positive terminal of an electronic load to the VDDQ post (J5). Connect the return terminal of the same load to the adjacent GND post (J7).

Loading V_{TT} - Sourcing Current: To test V_{TT} while the regulator sources current, connect the positive terminal of an electronic load to the VTT post (J6). Connect the return terminal of the same load to the adjacent GND post (J9).

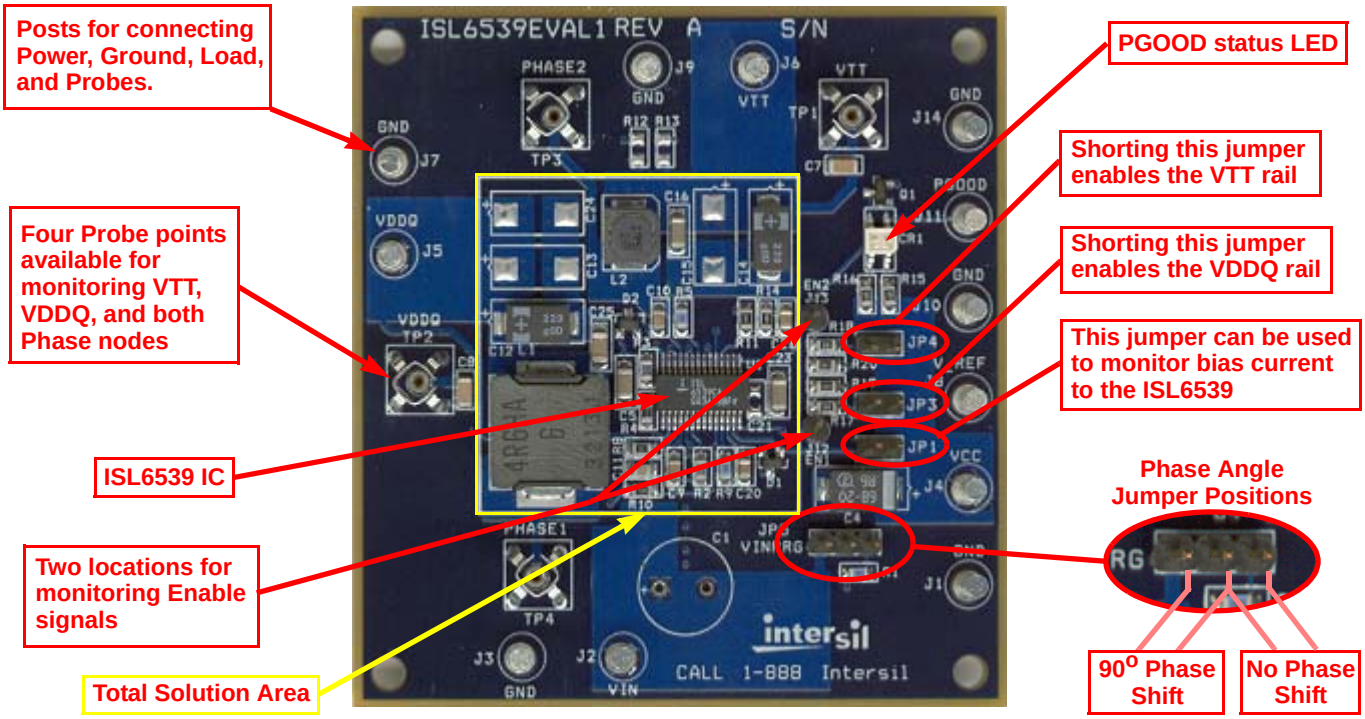


FIGURE 1. ISL6539EVAL1 BOARD

Loading V_{TT} - Sinking Current: To test V_{TT} while the regulator sinks current, connect the positive terminal of an electronic load to the VDDQ post (J5). Connect the return terminal of the same load to the VTT post (J6).

CAUTION: The return terminal of the load must float for this to work properly.

CONNECTING PROBES

The table below lists all the locations available for monitoring. The scope probe test points provide a low impedance ground connection and all GND post can be utilized as a ground connection for probes.

TYPE	VOLTAGE	LOCATION
POST	V_{DDQ}	J5
	V_{TT}	J6
	V_{PGOOD}	J11
	V_{REF}	J8
	V_{CC}	J4
	V_{IN}	J2
SCOPE PROBE TEST POINT	V_{TT}	TP1
	V_{DDQ}	TP2
	V_{PHASE1}	TP4
	V_{PHASE2}	TP3
TERMINAL	V_{EN1}	J12
	V_{EN2}	J13

TABLE 2. PROBE TYPES AND LOCATIONS

Terminals J12 (EN1) and J13 (EN2) may also be connected to a pulse generator for controlled ON/OFF operation of the respective regulators. However, make sure the signal generator for the enable voltage is no more than 5V and that the respective Enable jumper is removed.

CONNECTING POWER

Prior to connecting the power supplies to the evaluation board, the power supplies should either be turned off or the outputs should be disabled.

VCC Power Connection: Connect the positive terminal of a laboratory power supply to the VCC post (J4). Connect the return terminal of the same load to the adjacent GND post (J1).

V_{IN} Power Connection: Connect the positive terminal of a laboratory power supply to the VIN post (J2). Connect the return terminal of the same load to the adjacent GND post (J3).

Operation

APPLY POWER

Prior to applying power, ensure that jumpers JP1 and JP5 are in the desired position, all loads are connected properly, and all probes are connected properly. Jumpers JP3 and JP4 can be shunted and removed after power has been applied.

The V_{IN} power supply must be turned on or enabled first. Likewise, it must always be disabled or turned off last. This supply can be set from a minimum of $1.2V_{DDQ}$ to a maximum of 18V. After the V_{IN} power supply has been enabled, the VCC power supply may be enabled. The VCC power supply must be 5V.

The PGOOD status LED will give a visual indication of the V_{DDQ} regulator level. Table 3 describes the two states of the LED.

LED	CONDITION	RESULT
CR1	Green	V_{OUT1} WITHIN PGOOD RANGE (89%-115% of nominal value)
	Red	V_{OUT1} OUTSIDE PGOOD RANGE (89-115% of nominal value)

TABLE 3. PGOOD STATUS LED CONDITION INDICATOR

EXAMINE WAVEFORMS

Start-up is immediate following Power On Reset (POR). Using an oscilloscope or other laboratory equipment, the ramp-up and/or regulation of the outputs can be studied. Loading of the outputs can be accomplished through the use of electronic loads. Any other method, however, will work as well.

Evaluation Board Design

General

The evaluation board is built on a 2-ounce, four layer printed circuit board. The board is designed to support a continuous load of 5A on the V_{DDQ} rail and a simultaneous 3A continuous load on the V_{TT} rail while operating at room temperature and under natural convection cooling. Loading on V_{REF} should not exceed 10mA.

The schematic, bill of material, and the layout plots for the ISL6539EVAL1 evaluation board are provided at the end of this application note.

Eval Board Performance

Power-Up

When the V_{CC} voltage exceeds the POR level, the ISL6539 will begin the soft-start procedure. Figure 2 shows the start-up of both the V_{DDQ} and V_{TT} rails from POR.

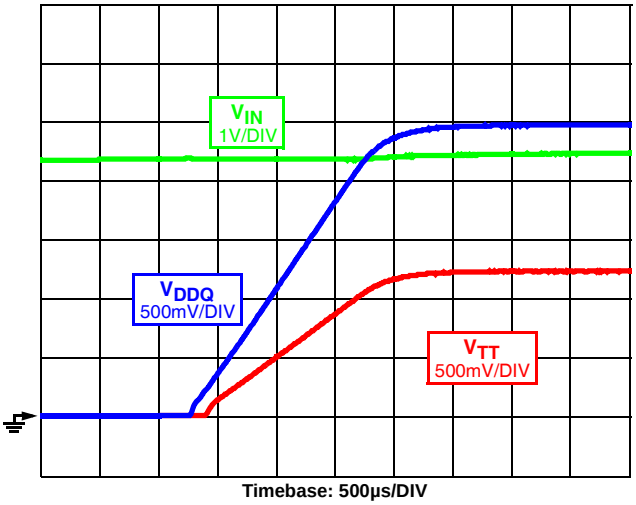


FIGURE 2. POR SOFT-START, VCC = VIN

Figure 3 shows the start up the V_{DDQ} and V_{TT} rails through the enabling of the V_{DDQ} regulator.

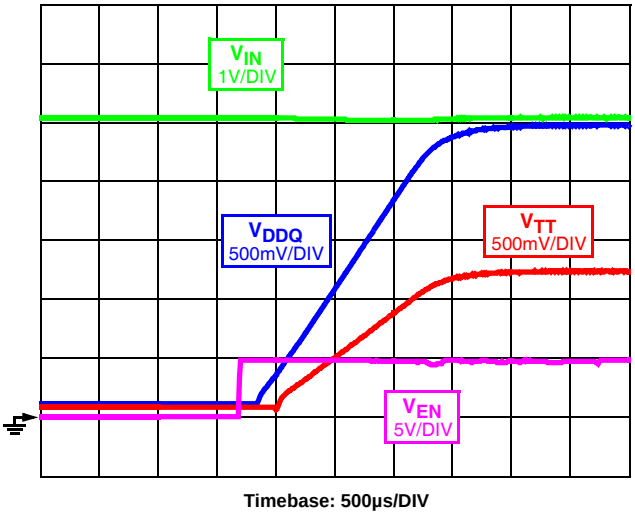
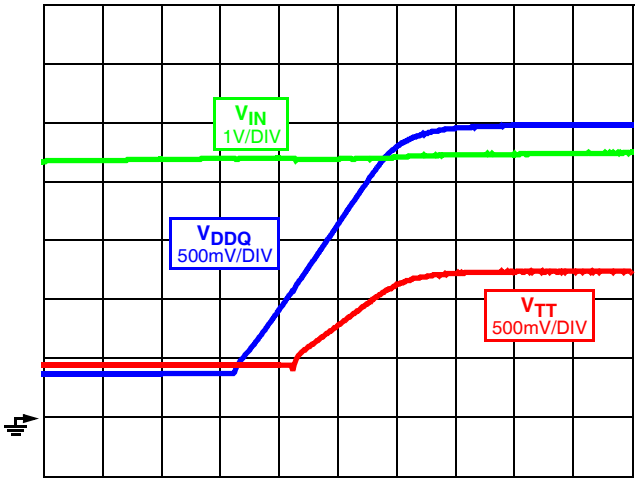


FIGURE 3. ENABLED SOFT-START

The ISL6539 is capable of starting into a prebiased output rail. Figure 4 shows the ISL6539 soft-starting both the V_{DDQ} and V_{TT} rails from POR with a prebias on the V_{DDQ} rail.

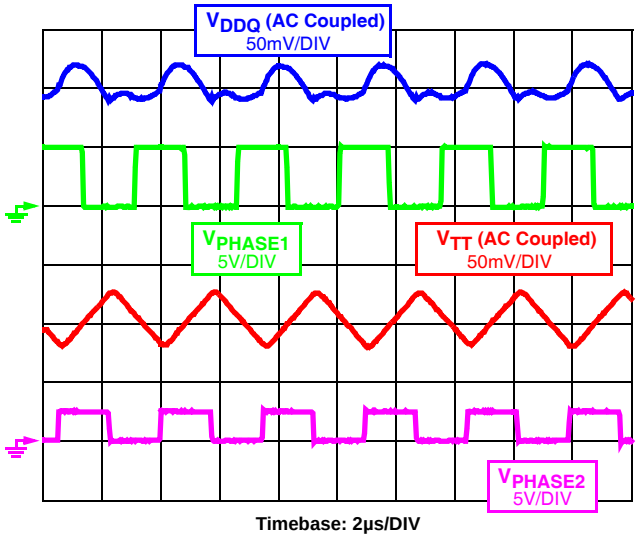


Timebase: 500µs/DIV

FIGURE 4. START-UP INTO PREBIASED OUTPUT

Output Ripple

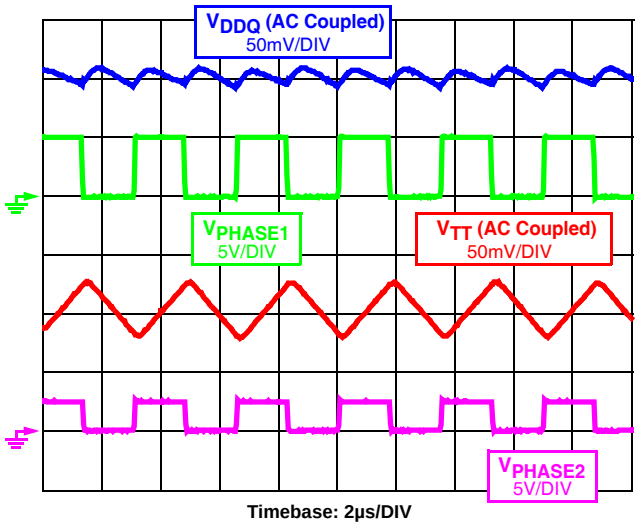
Figure 5 shows the ripple on both the V_{DDQ} and V_{TT} rails with a 90° phase shift implemented between the two regulators.



Timebase: 2µs/DIV

FIGURE 5. OUTUPT RIPPLE - 90° PHASE SHIFT

Figure 6 shows the ripple on both the V_{DDQ} and V_{TT} rails with a no phase shift implemented between the two regulators.

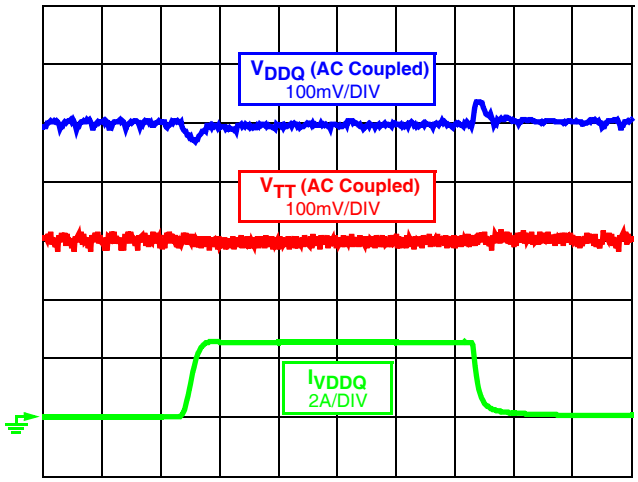


Timebase: 2µs/DIV

FIGURE 6. OUTUPT RIPPLE - NO PHASE SHIFT

Transient Performance

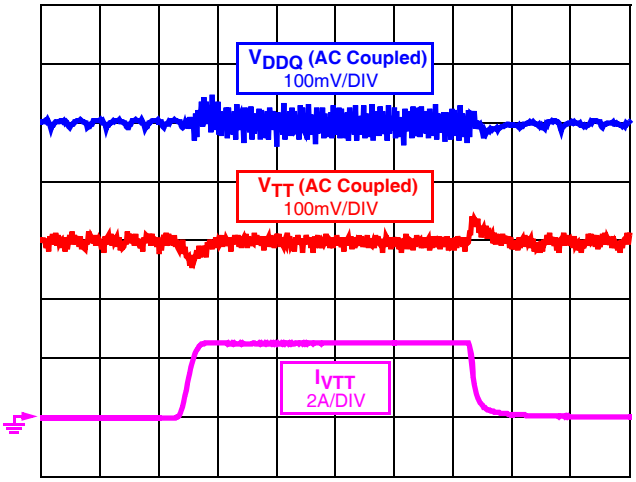
Figure 7 shows both the V_{DDQ} and V_{TT} rails while the V_{DDQ} rail is under transient loading.



Timebase: 100µs/DIV

FIGURE 7. TRANSIENT LOAD ON V_{DDQ}

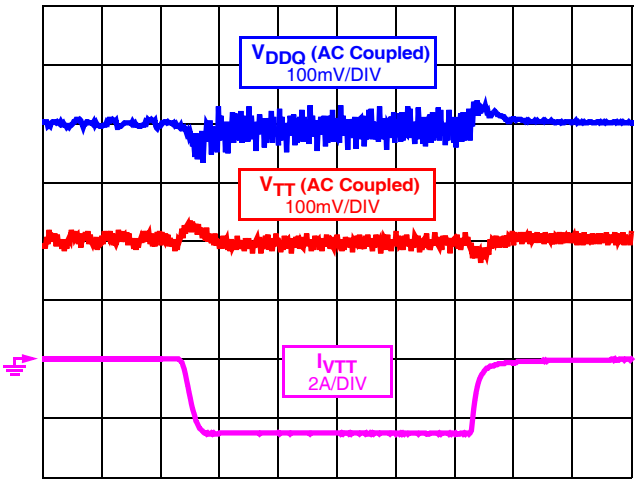
Figure 8 shows both the V_{DDQ} and V_{TT} rails while the V_{TT} rail is experiencing a sourcing transient load.



Timebase: 100µs/DIV

FIGURE 8. SOURCING TRANSIENT LOAD ON V_{TT}

Figure 9 shows both the V_{DDQ} and V_{TT} rails while the V_{TT} rail is experiencing a sinking transient load.



Timebase: 100µs/DIV

FIGURE 9. SINKING TRANSIENT LOAD ON V_{TT}

Efficiency

Figure 10 shows the efficiency of the individual regulators. These efficiencies were measured while the complementary regulator was disabled.

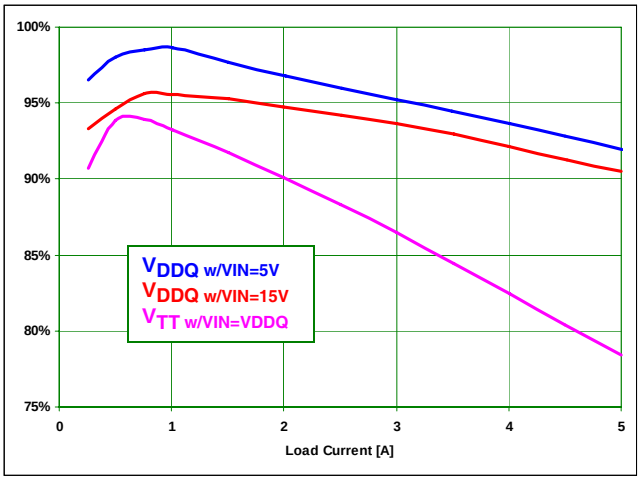


FIGURE 10. EFFICIENCY

ISL6539EVAL1 Customization

There are numerous ways in which a designer might modify the ISL6539EVAL1 evaluation board for differing requirements. Some of the changes which are possible include:

- The output inductors, L1 and L2, for the V_{DDQ} and V_{TT} regulators, respectively.
- The input capacitance may be changed. The evaluation board is shipped with two 10µF ceramic capacitors, C2 and C3, as the input capacitance. A spot has been set aside for the installation of a 10mm diameter through hole aluminum electrolytic capacitor in location C1.
- The output capacitance of either regulator may be modified. The evaluation board is shipped with one 220µF capacitor on the output of each regulator. There are two empty locations, C13 and C24, available for the V_{DDQ} regulator and one empty location, C15, available for the V_{TT} regulator.
- The overcurrent trip point of the V_{DDQ} regulator, programmed through the OCSET resistor, R9. Refer to the ISL6539 datasheet for details on this.
- Changing the value of C20 will alter the rise time of the outputs during soft-start. Refer to the ISL6539 datasheet for details on this.
- The load capacity for either rail can be increased by exchanging the MOSFETs, U2 and U3, for ones with higher current handling capabilities. The ISEN resistor values, R4 and R5, may need to be modified if this is done. The overcurrent resistor value, R9, would also have to be reviewed. Refer to the ISL6539 datasheet for details on calculating the values of these resistors.
- The output voltage of the V_{DDQ} regulator may be modified by changing resistor R10. Refer to the ISL6539 datasheet for details on this.
- The percentage at which the V_{TT} rail and the V_{REF} voltage track the V_{DDQ} rail can be modified by altering the resistor divider set up by resistors R11 and R14.

Conclusion

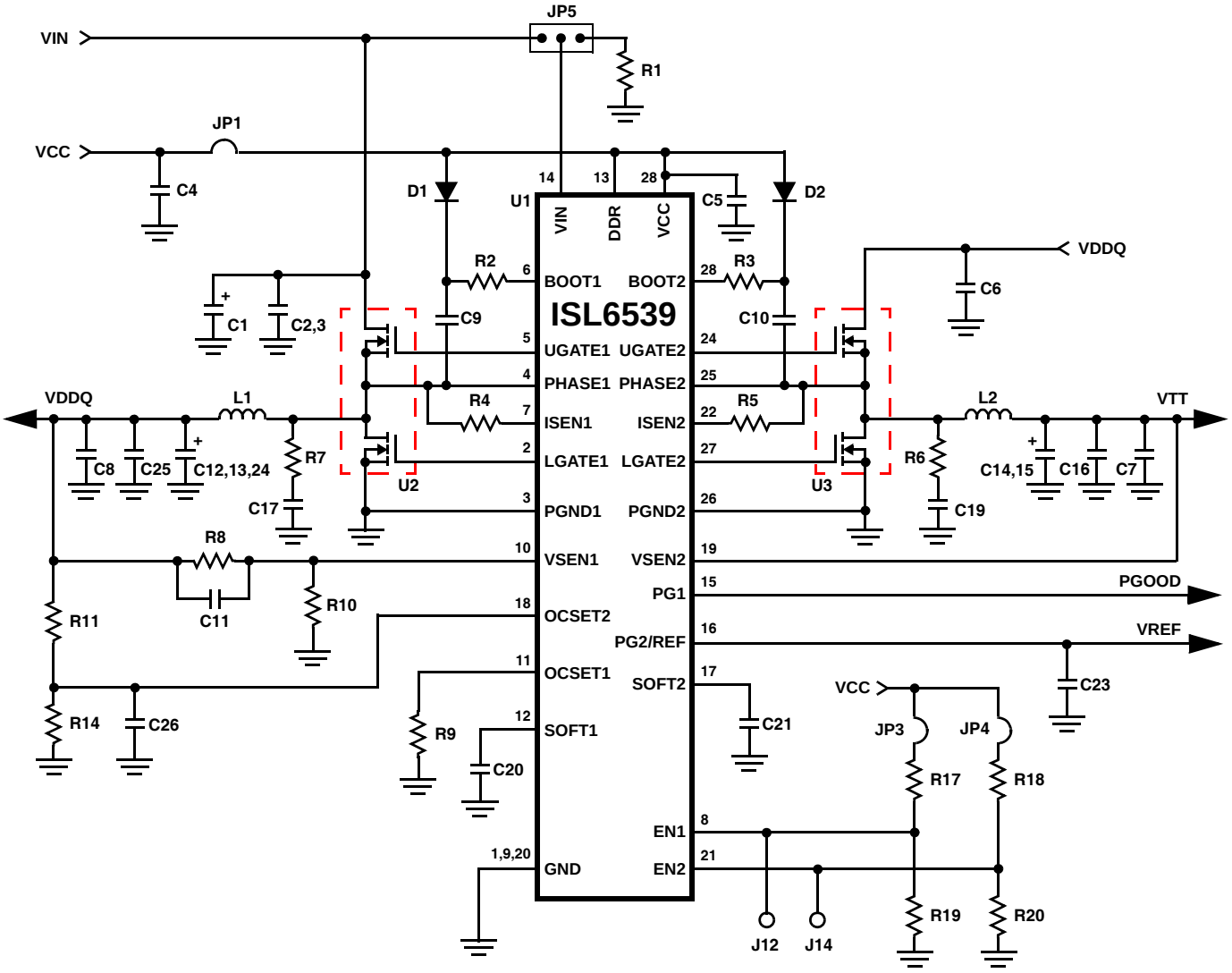
The ISL6539EVAL1 is a versatile platform that allows designers to gain a full understanding of the functionality of the ISL6539 in a DDR memory system. The board is also flexible enough to allow the designer to modify the board for differing requirements. The following pages provide a schematic, bill of materials, and layout drawings to support implementation of this solution.

References

For Intersil documents available on the web, see http://www.intersil.com/

[1] *ISL6539 Data Sheet,* Intersil Corporation, File No. FN9144.

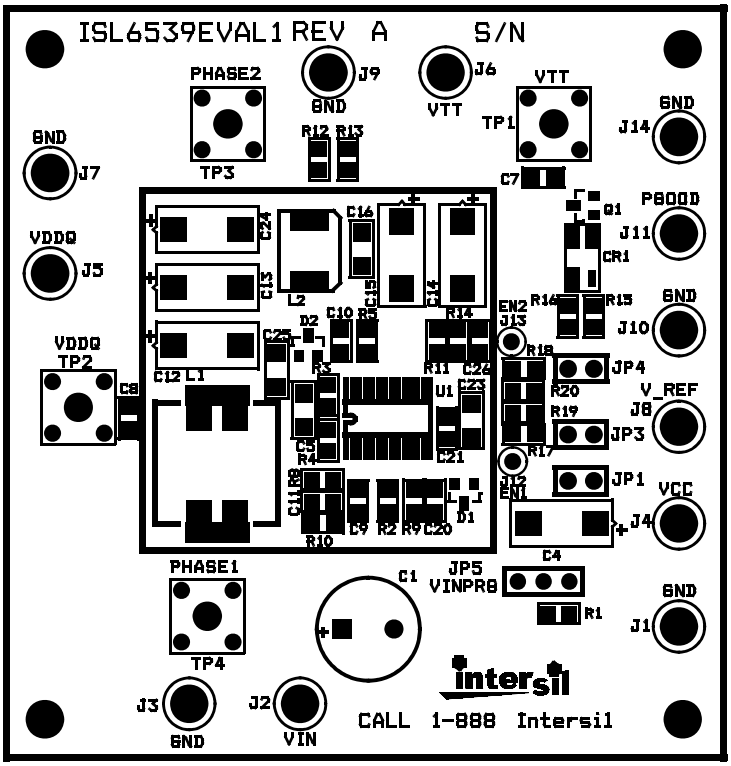
ISL6539EVAL1 Schematic



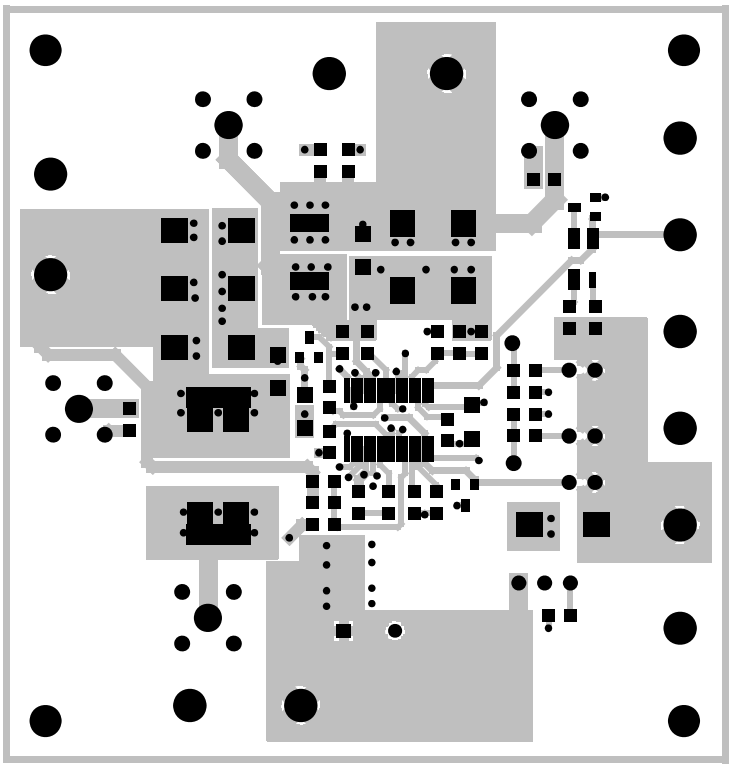
ISL6539EVAL1 Bill of Materials (BOM)

QTY	REFERENCE	DESCRIPTION	VENDOR	MFG. PART NO.
2	C20, C26	CAPACITOR, SMD, 0805, 0.01µF, 50V, 10%, X7R	PANASONIC	ECJ-2VB1H103K
1	C11	CAPACITOR, SMD, 0805, 0.015µF, 50V, 10%, X7R	PANASONIC	ECU-V1H153K
2	C9, C10	CAPACITOR, SMD, 0805, 0.15µF, 25V, 10%, X7R	PANASONIC	ECJ-2YB1E154kK
2	C7, C8	CAPACITOR, SMD, 1206, 1µF, 10V, 10%, X7R	VENKEL	C1206X7R100-105KNE
5	C5, C6, C16, C23, C25	CAPACITOR, SMD, 1206, 4.7µF, 10V, 10%, X7R	VENKEL	C1206X7R100475KNE
3	C12, C13, C14, C24	CAP TANT, LOW ESR, SMD, D3, 220µF, 4V, 20%	SANYO	4TPC220M
1	C4	CAP TANT, LOW ESR, SMD, D, 68µF, 16V,10%	KEMET	T494D686K016AS
2	C2, C3	CAPACITOR, SMD, 1812, 10µf, 25V, 20%, X5R	TAIYO YUDEN	TMK432BJ106MM-T
2	D1, D2	DIODE-SCHOTTKYBARR, SMD, SOT323, 3P, 30V, 0.2A	ON-SEMICONDUCTOR	BAT54WT1-T
1	CR1	LED, SMD, 4P, OTHER, POLARIZED RED/GRN	LUMEX	SSL-LXA3025IGC-TR
1	L1	PWR CHOKE COIL, SMD, 5.7mm, 4.6µH, 25%	PANASONIC	ETQ-P6F4R6HFA
1	L2	PWR CHOKE COIL, SMD, 6x6x3mm,1.5µH, 20% 3.2A	PANASONIC	ELL6SH1R5M
1	U1	IC-DUAL SWITCHER 30V, 28P, QSOP	INTERSIL	ISL6539CA
1	Q1	TRANSISTOR, N-CHANNEL, 3P, SOT23	ON-SEMICONDUCTOR	BSS123LT1-T
2	U2, U3	TRANSISTOR - DUAL MOS, N-CHANNEL, 8P, SOIC, 30V	FAIRCHILD	FDS6912A
2	R2, R3	RESISTOR, SMD, 0805, 0Ω, 1/10W, TF	PANASONIC	ERJ-6GEY0R00V
1	R5	RESISTOR, SMD, 0805, 1k, 1/10W, 1%, TF	PANASONIC	ERJ-6ENF1001
5	R10, R11, R14, R19, R20	RESISTOR, SMD, 0805, 10k, 1/10W, 1%, TF	PANASONIC	ERJ-6ENF1002V
2	R1, R9	RESISTOR, SMD, 0805, 100k, 1/10W, 1%, TF	PANASONIC	ERJ-6ENF1003V
1	R8	RESISTOR, SMD, 0805, 17.8k, 1/10W, 1%, TF	PANASONIC	ERJ-J6ENF1782V
1	R4	RESISTOR, SMD, 0805, 2.49k, 1/10W, 1%, TF	PANASONIC	ERJ-6ENF2491
4	R15 - R18	RESISTOR, SMD, 0805, 680Ω, 1/10W, 5%, TF	PANASONIC	ERJ-6GEYJ681V

ISL6539EVAL1 Printed Circuit Board Layers

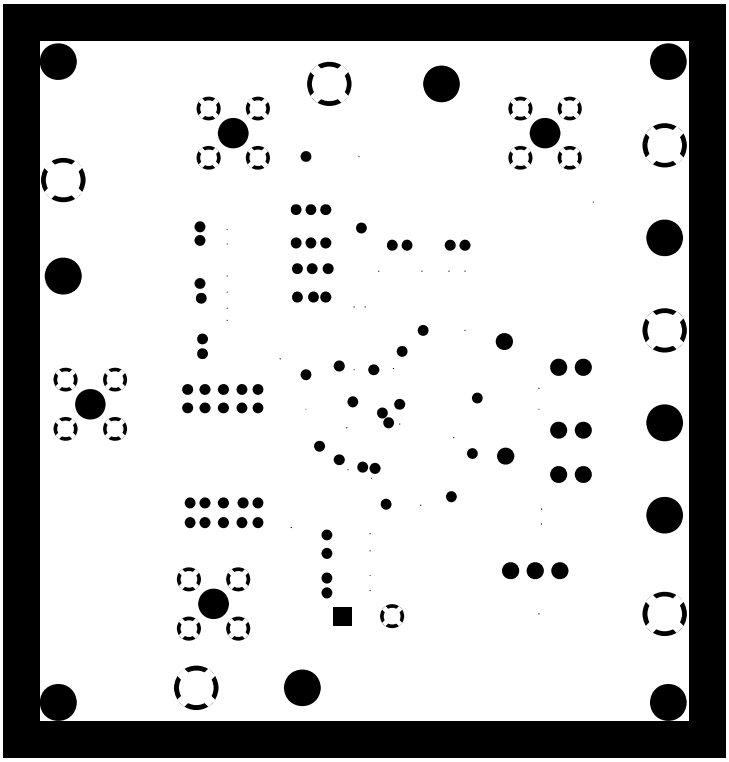


ISL6539EVAL1 - TOP SILK SCREEN

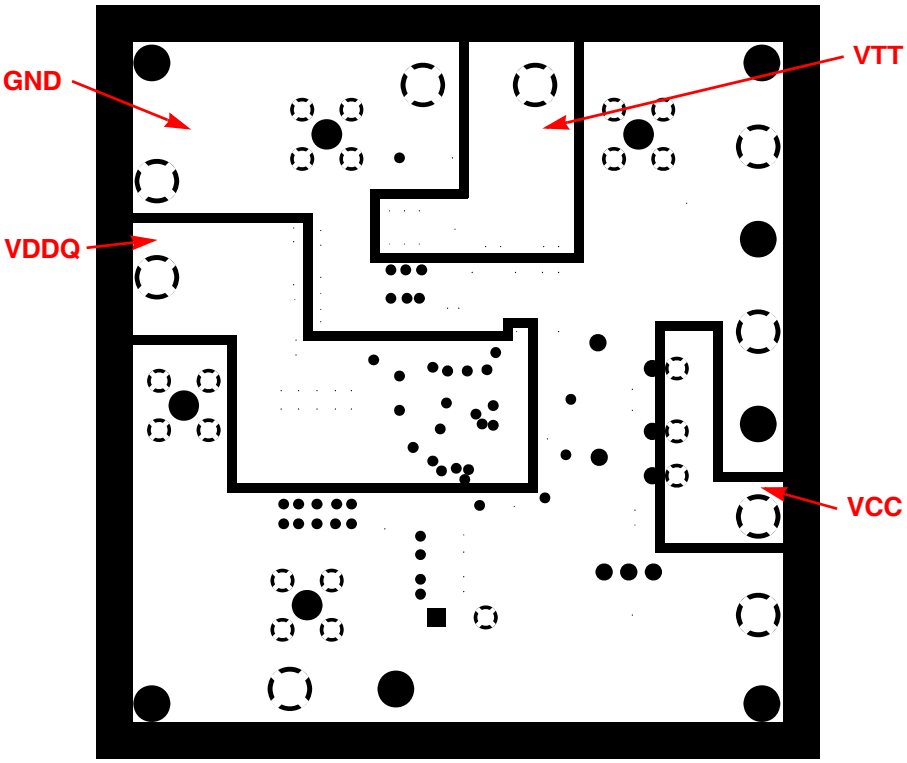


ISL6539EVAL1 - TOP LAYER

ISL6539EVAL1 Printed Circuit Board Layers (Continued)

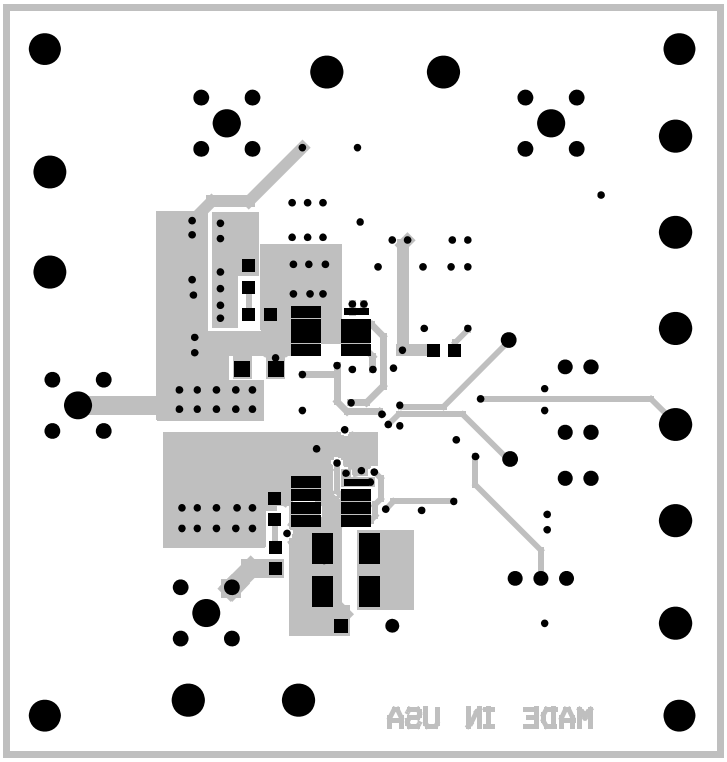


ISL6539EVAL1 - INTERNAL 1 - GROUND

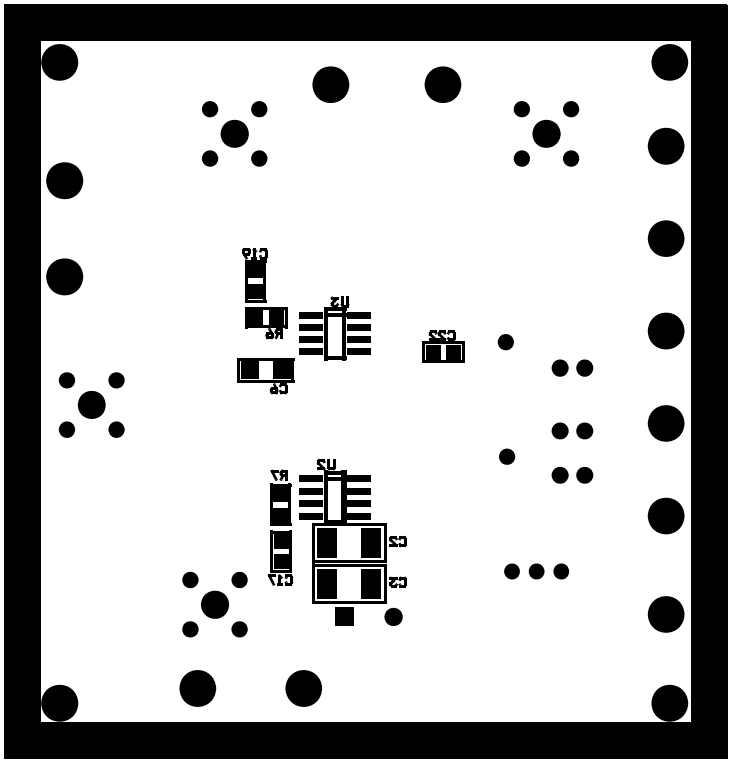


ISL6539EVAL1 - INTERNAL 2 - POWER

ISL6539EVAL1 Printed Circuit Board Layers (Continued)



ISL6539EVAL1 - BOTTOM LAYER



ISL6539EVAL1 - BOTTOM SILK SCREEN