

ITS4880R

Octal Smart Power High-Side-Switch for Industrial Applications

Errata Sheet

Rev.1.0, 2014-10-10

Standard Power



Rev.1.0, 2014-10-10

ITS4880R Octal Smart Power High-Side-Switch for Industrial Applications

Reference: ITS4880R Data Sheet Rev. 1.1

Overview

This document lists the errata of the ITS4880R in relation to the ITS4880R Data Sheet Rev. 1.1 Evaluation and listed points are still under investigation.

1 Description

The functionality of the LS pin (Pin 3) for the ITS4880R as described in Data Sheet Rev. 1.1 on page 9 is valid for static conditions. Determined by the high impedance of the LS-pin and the capacitance of the LS-protection to $V_{\rm BB}$, the functionality can be affected by high slew rates on $V_{\rm BB}$. In order to avoid this, the LS pin should not be left open and should be connected either to GND or to supply voltage. If the LS pin is connected to the supply voltage $V_{\rm BB}$ the input threshold is set to 50% of $V_{\rm BB}$. Connecting the LS pin to GND sets the input threshold to CMOS levels.

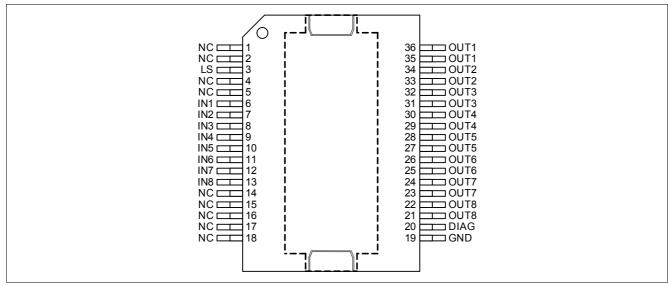


Figure 1 Pin configuration ITS4880R, PG-DSO-36

2 Planned Fixes

Change in Data Sheet: Changes will be made as described below under the section 'Functional Description LS-Pin' of the ITS4880R Datasheet Rev.1.1.

2.1 Functional description LS-Pin

The following statement in the datasheet: 'If the LS-pin is not connected the input threshold voltages are automatically at CMOS levels' is valid for static conditions. Depending on the slew rate at $V_{\rm BB}$, the internal network with $R_{\rm LS-GND}$ which is typically $800 {\rm k}\Omega$ causes a voltage overshoot on LS, which might lead consequentialy (due to



Planned FixesReference: ITS4880R Data Sheet Rev. 1.1

parasitics) to a permanent deviation of the described LS-pin behavior (voltage level between CMOS and $V_{\rm BB}/2$ levels).

Edition 2014-10-10

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